**I. COURSE TITLE:** Digital Electronics

**COURSE NUMBER:** 2205  **CATALOG PREFIX:** EENG

**II. PREREQUISITES:** EENG 1105 coreqiusite equivalent

**III. CREDIT HOURS:** 3 **LECTURE HOURS:** 2

**LABORATORY HOURS:** 1**(**2 contact) **OBSERVATION HOURS:** 0

 **IV. COURSE DESCRIPTION:**

An examination of number systems and techniques of logical reduction. Pulse and logic circuits, counters, registers, logic families, integrated circuits and basic elements of digital design are discussed. Including DA & AD convertors microprocessor & microcontrollers.

**V. GRADING:**

Grading will follow the policy in the school catalog.

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **90** | **–** | **100** |
| **B** | **80** | **–** | **89** |
| **C** | **70** | **–** | **79** |
| **D** | **60** | **–** | **69** |
| **F** | **0** | **–** | **59** |

**VI. ADOPTED TEXT(S):**

 *Digital Electronics****-****A Practical Approach*

9th Edition

William Kleitz.

 **P**rentice-Hall

 ISBN: 0-13-254303-6

**VII. COURSE OBJECTIVES:**

Number systems, operations and codes\*

1. Logic gates\*
2. Boolean Algebra \*
3. DeMorgan’s theorem and logic simplification\*
4. Combinational logic circuits\*
5. Encoders/decoders\*
6. Multiplexers/demultiplexers\*
7. Adders, subtractors, ALUs\*
8. Flip-flops and related devices\*
9. Counters\*
10. Shift registers\*
11. Memory and storage\*
12. Integrated circuit technologies\*
13. Introduction to micoprocessors & microcontrollers
14. VHDL Topics

**VIII. COURSE METHODOLOGY**

Learning objectives will be taught by lectures, labs videos, plant visits or any method which is effective in teaching the material.

**IX. COURSE OUTLINE:**

**WEEK**

1. CH 1, 2,& 3

Numbering systems

 Digital Signals

 Basic Logic Gates

1. CH 1,2, & 3 (Cont) LAB 1

 AND, OR, NOR,

 INVERTERS

1. CH 4 & 5 TEST CH1-3

Programmable Devices

Boolean Algebra

4 CH 4 & 5 TEST CH 4-5

Programmable Devices

Boolean Algebra

5 CH 7 LAB 3

 Arithmetic circuits

6 CH 8

Code Converters, Muxs, DeMux TEST CH6-7

7 CH 9 TEST CH 8

Logic Families

8 CH 1O TEST CH 9

Flip-Flops & Registers LAB

9 CH 11 TEST 10-11

 Practical design considerations

10 CH 12, 13

Counters Shift Registers & VHDL

11 CH 14

 Multivibrators, 555 Timer Lab 555

12 CH 15

 Interfacing Analog

13. CH 16

 Memory

14 CH 17

 Microprocessor fundamentals

15 CH 18

 Microcontollers

16 **Final**

**X. OTHER BOOKS, SOFTWARE AND MATERIALS:**

Scientific Calculator, $40 Lab Fee for instrumentation & materials

**XI. EVALUATION:**

Test = 40% - 10% for unexcused absences

 Lab = 40% - 10% for unexcused absences

Final = 20%

**XII. SPECIFIC MANAGEMENT REQUIREMENTS:**

None

**XIII. OTHER INFORMATION**

**FERPA:** Students need to understand that your work may be seen by others. Others may see your work when being distributed, during group project work, or if it is chosen for demonstration purposes.

 Students also need to know that there is a strong possibility that your work may be submitted to other entities for the purpose of plagiarism checks.

 **DISABILITIES:** Students with disabilities may contact the Disabilities Service Office, Central Campus, at 800-628-7722 or 937-393-3431.